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EUROCOM (D/1) Data Class 3 Clock Regeneration Implementation

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ABSTRACT (UNCLASSIFIED)

This report describes the development of a EUROCOM DATA Class 3, clock regeneration implementation, as part of FEL/TNO's support to the Royal Netherlands Army (RNLA), ZODIAC project. The design is based on the use of a Digital Phase Locked Loop (DPLL) which recovers a stable 2.4 kHz clock with a jitter content of between 1-2%, from the received multi-sampled majority voted signal in the presence of a bearer circuit error rate of 1 in 10^2, as specified in EUROCOM (D/1).

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SAMENVATTING (ONGERUBRICEERD)

Dit rapport beschrijft de ontwikkeling alsmede de implementatie van een 'EUROCOM DATA Class 3' klokregenerator. Dit onderzoek is uitgevoerd door het FEL/TNO in het kader van het ZODIAC project. Het ontwerp is gebaseerd op een digitale PLL. Deze digitale PLL wordt gebruikt om een stabiel 2.4 kHz kloksignaal op te wekken (jitter 1-2%) uitgaande van het 'multi-sampled majority voting' (MSMV) bemonsterde ontvangen signaal. Hierbij is in het ontvangen signaal een Bit Error Rate (BER) van 10^{-2} toegelaten zoals in EUROCOM (D/1) is gepecificeerd.

1 INTRODUCTION

Within the EUROCOM Tactical Communications Systems, Basic Parameters (D/1), specification, [Ref 1], facilities are provided for the transmission of non-voice traffic, such as computer to computer or computer to peripheral, telegraph and facsimile, within the Trunk Node Network (TNN). This "DATA", as it is defined in EUROCOM (D/1), can operate either anisochronous[1] or isochronous[1] in signal structure, asynchronous[1] or synchronous[1] with the bearer circuit timing, as well as at different bit rates. Before being transmitted over the bearer circuit the DATA is subjected to different processing and error detection/correction principles so as to meet the stipulated DATA integrity requirements. The type of processing to be implemented on the DATA depends on its classification as shown in Table 1.

CLASS	STRUCTURE	PHASE RELATION WITH BEARER CIRCUIT	PROCESSING
1	ISOCHRONOUS	SYNCHRONOUS	NONE
2	ANISOCHRONOUS	ASYNCHRONOUS	MSMV
3	ISOCHRONOUS	ASYNCHRONOUS/ SYNCHRONOUS	MSMV&R
4	ISOCHRONOUS	SYNCHRONOUS	FEC

MSMV: Multiple Sampling and Majority Voting
MSMV&R: Multiple Sampling and Majority Voting and Regeneration
FEC: Forward Error Correction using Block Code

Table 1.: DATA Classes

This report shall concentrate only on Class 3 and the 'Regeneration' section. The other classes are fully defined in EUROCOM (D/1).

1: **For a full definition of these terms as used in EUROCOM (D/1), refer to Chapter IA General Characteristics, Section 9 para 1.**

2 DATA CLASS 3 PROCESSING

The following paragraphs give a brief description of DATA Class 3 processing. For those people that are familiar with DATA Class 3 it is probably not necessary to read this section.
The block diagram of a Data Circuit Terminating Equipment, (DCE), implementing Class 3 processing is shown in Figure 1. The Data Terminating Equipment, (DTE,) transmits to the DCE, isochronous data at a bit rate of 2.4 kbit/s, either asynchronous to the bearer circuit by using its own internal timing or synchronous to the bearer circuit by using the Transmitter Signal Element Timing, which the DCE derives from the bearer circuit timing. In both cases the Transmitted Data is sampled at the bearer circuit bit rate before being further processed, (i.e. code conversion) and transmitted over the bearer circuit.
At the receiving side of the DCE, the received bearer circuit signal, after any necessary decoding, is passed through a Running Majority Voting Detector, (RMVD), so as to reduce minor bit errors and regenerate the original 2.4 kbit/s data. From this regenerated 2.4 kbit/s data a recovered 2.4 kHz clock is generated which is transmitted to the DTE as the Received Signal Element Timing and is used to re-sample the regenerated 2.4 kbit/s data.

2.1 DATA Class 3 Multiple Sampling and Majority Voting

To give an understanding as to some of the problems involved in clock regeneration in DATA Class 3 a brief description of the Multiple Sampling and Majority Voting (MSMV) techniques used in this class are given below.
As stated before, the DTE's 2.4 kbit/s data is sampled at the bearer circuit bit rate, which in accordance with EUROCOM (D/1) operates at 16 kbit/s. The result of this sampling technique has two effects on the DTE Transmitted Data. The first effect results in a frequency offset of the 2.4 kbit/s, however over a long sample this is insignificant and therefore it can be ignored.

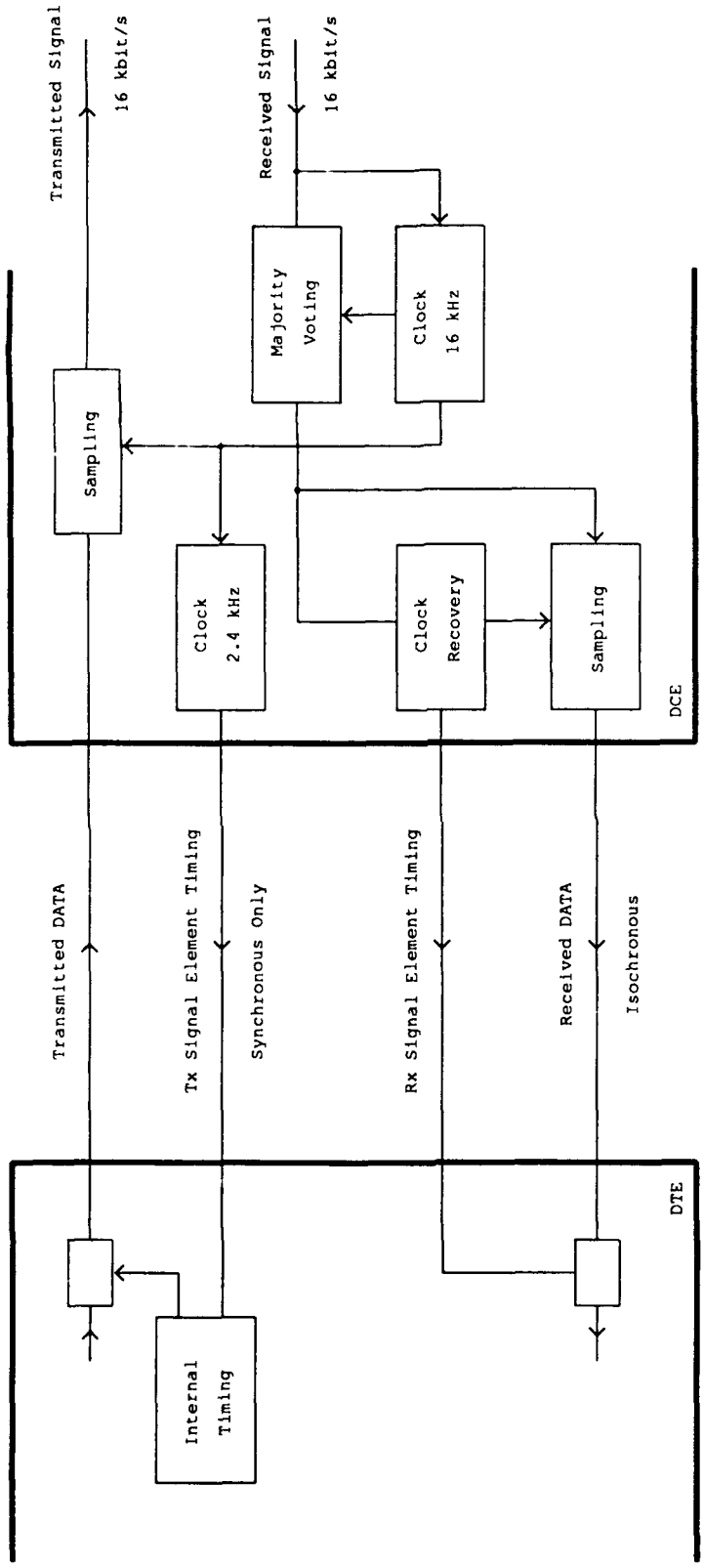


Fig. 1: Block Diagram of DATA Class 3 Processing

The second effect is the introduction of 'jitter' to the Transmitted Data for the following reason:
2.4 kHz is not an exact sub-multiple of 16 kHz and therefore when the 2.4 kbit/s Transmitted Data is sampled by the 16 kHz bearer circuit clock, an individual Transmitted Data bit period is either sampled 7 times or 6 times and over a time period of 20 samples this results in an uneven sample pattern of 2 data bit periods of 7 samples + 1 data bit period of 6 samples, (See Figure 2). The 'missed sample' is repeated every 20 samples which introduces upto a measured value of 16% jitter, referenced to the original Transmitted Data, onto the sampled Transmitted Data and assuming an error free bearer circuit it is reproduced by the RMVD at the far end receiving side.

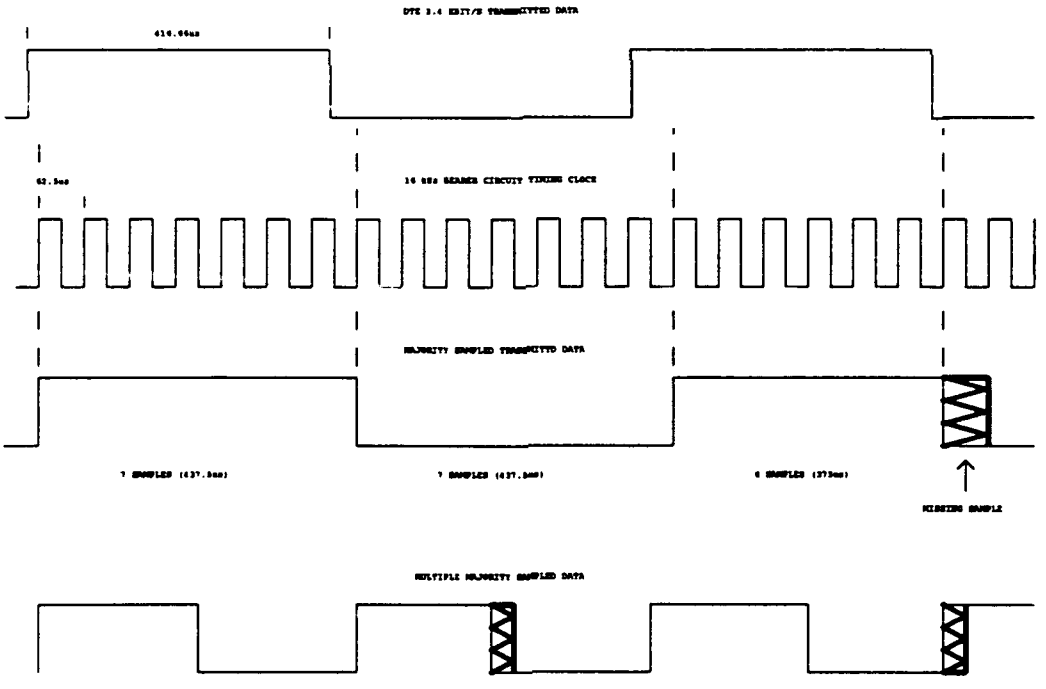


Fig. 2: Multiple Sampling Timing Diagram

In addition to the jitter introduced by the Multiple Sampling technique the Majority Voting technique can also introduce more jitter onto the regenerated 2.4 kbit/s data if there have been errors induced when transmitted over the bearer circuit. The RMVD operates such that it samples the received data over a 'window' length, in this case for 2.4 kbit/s, of 7 bit periods of the 16 kbit/s bearer circuit data, to determines whether there is a majority of logic 'ones' or 'zeros' over the 7 bit periods. The RMVD output then takes the value of the majority logic level and then it shifts along one 16 kbit/s bit period and repeats the process again, (See Figure 3).

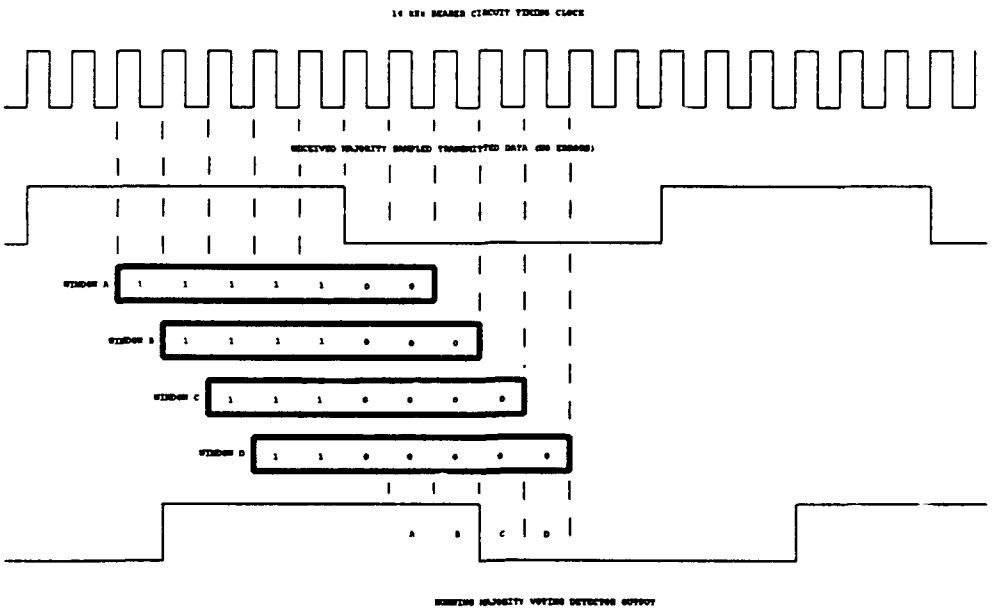


Fig. 3: Running Majority Voting Detection (No Errors)

If there were no errors introduced into the Transmitted Data bit period, when transmitted over the bearer circuit, then the output of the RMVD is the same as that of the Multiple Sampler. If there were errors introduced then the effect seen as a result of the RMVD error correction technique is, that Transmitted Data bit periods become shorter or longer. For example, if one error occurred in a 7 sample logic one

Transmitted Data bit period, the output of the RMVD, would be only 6 samples in length, (See Figure 4). This shortening and lengthening of the Transmitted Data bit periods has the effect of increasing the overall jitter content of the regenerated Received Data upto a measured value of 45%, referenced to the original DTE Transmitted Data, when an error rate of 1 in 10^2, as specified by EUROCOM, is experienced on the bearer circuit.

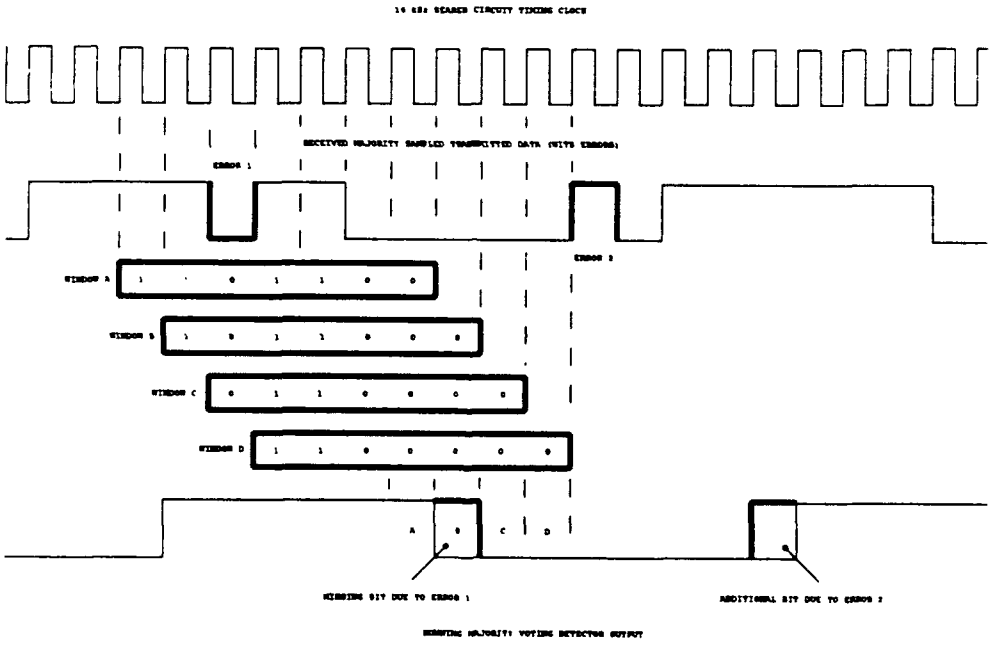


Fig. 4: Running Majority Voting Detection (With Errors)

3 DATA CLASS 3 CLOCK REGENERATION

EUROCOM DATA Class 3 processing requires that the DCE recovers a 2.4 kbit/s timing signal which is used to sample the RMVD output and be passed onto the DTE as the Received Signal Element Timing clock. Unlike most commercial DCE - DCE, (Modem - Modem), communication across a bearer circuit, where a timing element for the bit rate used is carried across the bearer circuit, in EUROCOM this is not the case and therefore the 2.4 kbit/s timing signal has to be recovered from the RMVD output signal. As already stated, this output signal contains varying amounts of jitter and also the DATA codes used between the DTEs, such as International Alphabet No. 5, (ITA 5), do not in principle contain any timing information as they can contain consecutive logic ones and zeros. The following description of a DATA Class 3 clock recovery implementation has be proven to be able to recover a stable 2.4 kHz timing clock from the RMVD output signal in the presence of a bearer circuit error rate as specified in EUROCOM (D/1).

3.1 Clock Recovery Implementation

A block schematic of the implemented DATA Class 3 Clock Recovery circuit is shown in Figure 5 and a circuit schematic in Figure 6. It primarily consists of four circuit areas, however, the Sampler circuit only re-times the output of the RMVD with the 'jitter free' recovered clock and therefore it will not be described below. The principle operation of the other areas are as follows:

3.1.1 Edge Detection Circuit

As stated previously the output signal of the RMVD has in principle no timing element information, however over a long sample period of random data it does have a fundamental frequency component of around 600 Hz. By feeding the RMVD output signal into the Edge Detection circuit, this fundamental frequency component is doubled as follows:
The RMVD output signal is re-sampled with a 38.4 kHz clock, derived from

the Digital Phase-Locked Loop (DPLL) circuit and this re-sampled RMVD output signal is passed through a one bit shift register. The outputs of the sampler and shift register are then exclusively OR'ed so as to produce a pulse train, where each pulse is 26.04us wide and occurs on every transition of the RMVD output signal. This pulse train now has a fundamental frequency component of around 1200 Hz (See Figure 6). This pulse train is then feed to the Counter circuit to be doubled once more.

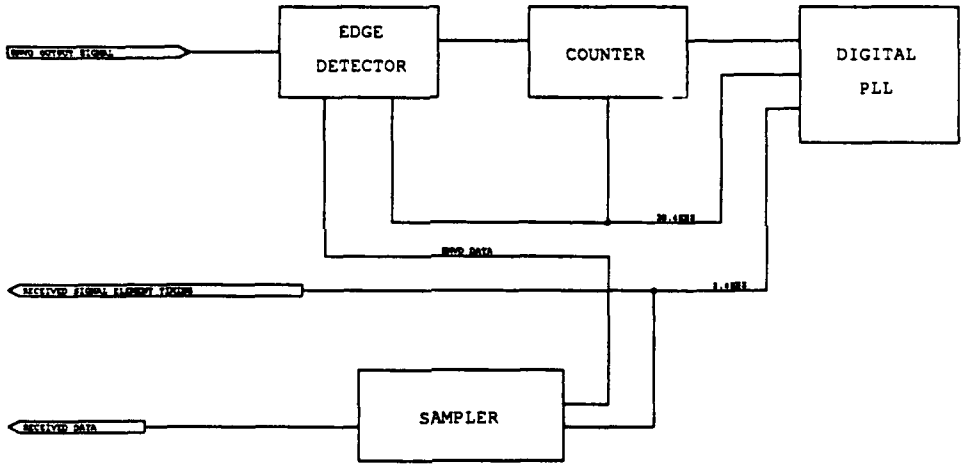


Fig. 5: Block Schematic of DATA Class 3 Clock Recovery Circuit

3.1.2 Counter Circuit

Although the RMVD output signal does not accurately represent the original DTE Transmitted Data, in that the length of the data bit periods in time are no longer an exact multiple of 2.4 kbit/s, due to the sampling jitter etc, every transition in the RMVD output signal does represent the same logical change in the original Transmitted Data.
It is this characteristic that is used to generate from the RMVD output signal a 2.4 kHz timing element input to the DPLL as follows:
The RMVD output signal transition pulses from the Edge Detector are used

to preset the value of a Counter which is also being clocked by the 38.4 kHz clock. The preset value chosen (i.e. 8) results in the output of the Counter circuit producing a pulse 208.33us in width from the start of every preset transition pulse, (See Figure 6). By producing the 208.33us pulse on ever transition of the re-sampled RMVD output signal the Counter circuit output produces a pulse train synchronous with the RMVD output signal and with a fundamental frequency of 2.4 kHz. This pulse train, however, still contains the jitter that was present on the RMVD output signal and therefore it is feed into the input of the Digital Phase Lock Loop (DPLL) so as to have the jitter removed.

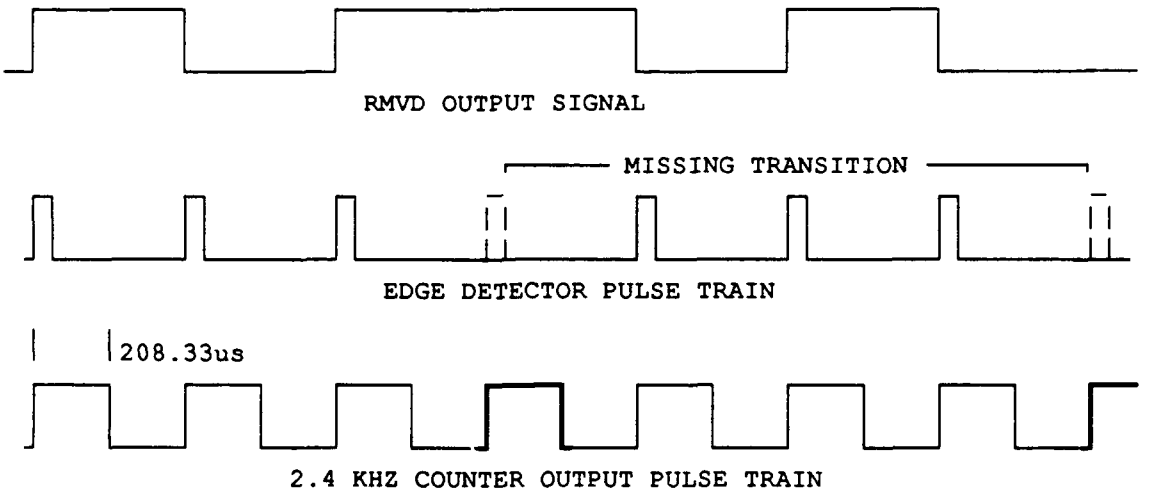


Fig. 6: Edge Detector and Counter Circuit Pulse Train Outputs

In the case where there are missing preset transition pulses, due to consecutive logic ones or zeros in the RMVD output signal, to maintain the pulse train the Counter circuit 'free-runs', producing a 208.33us pulse (bold) beginning at the next expected transition point in the RMVD output signal, timed from the last known actual transition point. In this way the Counter circuit continues to produce the 2.4 kHz pulse train as an input to the DPLL, in the absence of preset pulses, in phase with and having the same frequency as the last period of preset pulses.

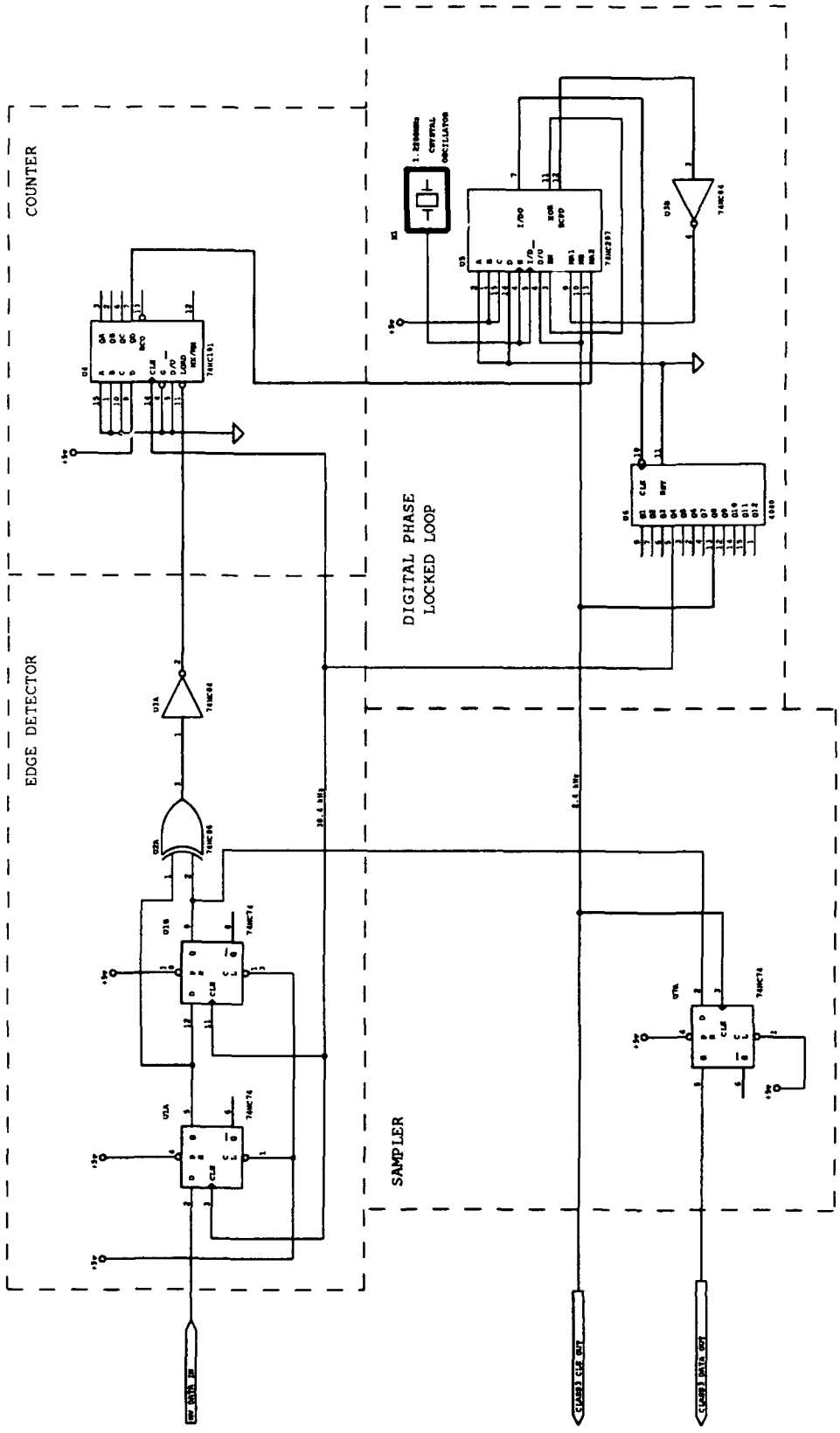


Fig. 7: Circuit Schematic of DATA Class 3 Clock Recovery Circuit

On the next actual transition in the RMVD output signal the Counter circuit is again preset and therefore is re-synchronised with the RMVD output signal.

3.1.3 Digital Phase Locked-Loop

As stated above the jittered 2.4 kHz pulse train output from the Counter circuit is applied to the input of the DPLL. The DPLL circuit consists of a reference clock (Mf_o) which is a 2^N multiple of the 2.4 kHz (f_o), a 74HCT297, [Ref. 2], and a +N counter. The 74HCT297 consists of a +K counter, Increment/Decrement (I/D) circuit and two phase detectors, Exclusive-OR'ed or Edge-controlled, (See Figure 8).

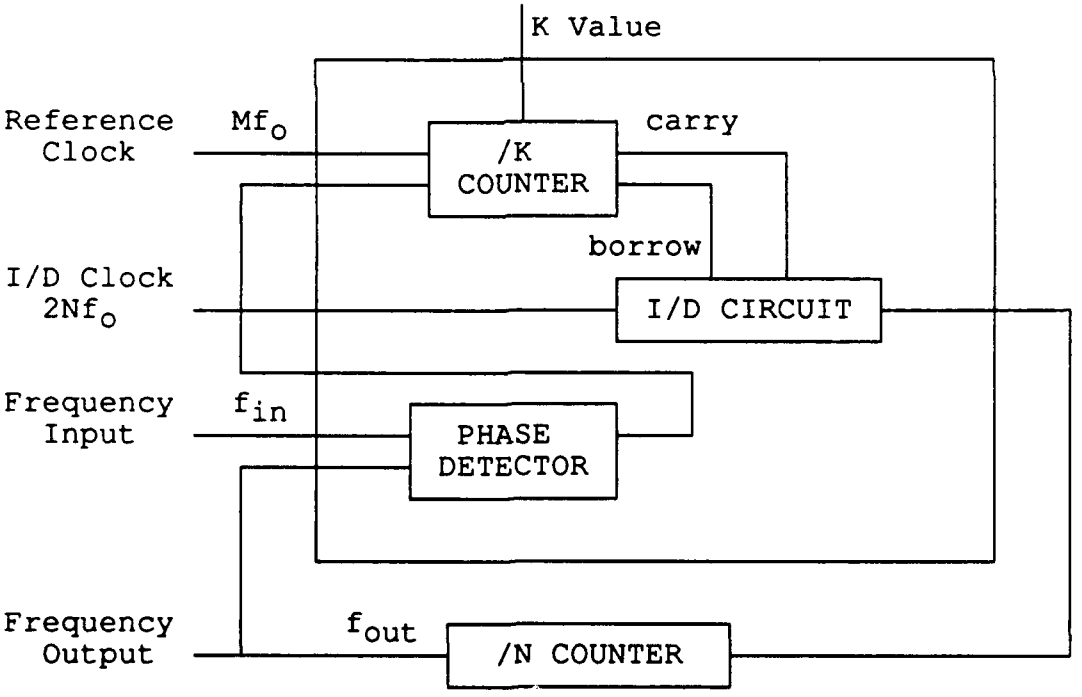


Fig. 8: 74HCT297 Digital Phase-Locked Loop

The operation of the 74HCT297 is, that the employed phase detector(s) compares the phase and frequency difference between the input signal (f_{in}) and the output signal (f_{out}) from the +N counter. The resultant

phase detector output signal then drives the up/down input of the +K counter. The reference clock samples the +K counter, which in turn produces a number of 'carry' or 'borrow', (i.e. inc. or dec.), pulses at its output, dependent on the input signal received from the phase detector and the selected value of K the counter variable These carry or borrow pulses are feed to the Increment/Decrement circuit, which is sampled at a clock rate of $2Nf_o$, where they add or delete respectively, pulses to/from the circuits output clock effectively increasing or decreasing the output centre frequency (See Figure 9)

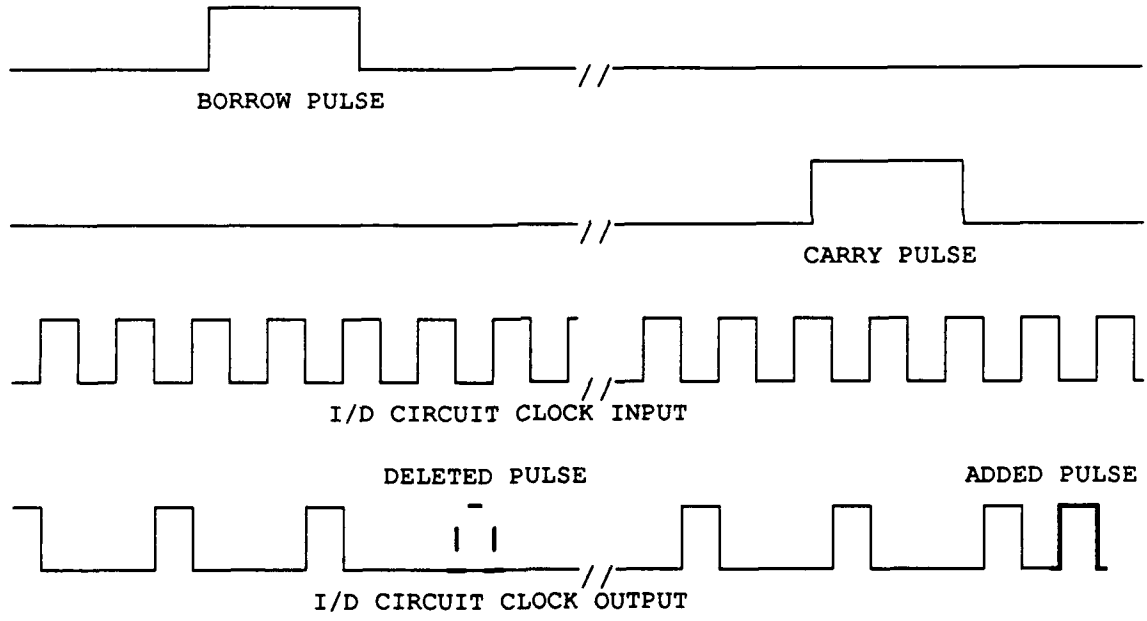


Fig. 9: I/D Circuit Timing Diagram

The output of the Increment/Decrement circuit is then feed to the input of the +N counter. In this manner the output frequency is continually adjusted so that when the loop is in lock ,(i.e. no carry or borrow pulses), the output frequency is in phase with, and equal in frequency to, the input frequency. The characteristics of the DPLL such as Lock Range, Capture Range and effective Q are primarily determined by the value K and the reference clock.

The configuration used in this DATA Class 3 Clock Recovery circuit employed a reference clock having a frequency of 1.2288 Mhz and a K value of 512 for the following reasons:
The resultant of the I/D circuit adding or deleting pulses to/from its output clock is that this clock in itself now contains ripple (i.e. jitter) and therefore to reduce the jitter on the final output clock to about 1% the +N counter must have a N value ≥100. Note the jitter value of 1% was a personal chose, as EUROCOM (D/1) does not specify any output jitter figure for the recovered Received Signal Element Timing.
The nearest 2^N multiple of 100 is 128, however as the circuit design also uses a 38.4 kHz clock, also derived from the I/D Circuit output clock which will also contain jitter, to reduce further the jitter on this clock and the final output clock the value of N chosen was 256. Using this value of N the I/D output clock Nf_o = 256*2400 = 614.4 kHz. When the DPLL is in lock the I/D Circuit acts simply as a +2 function and therefore the I/D Circuit input clock $2Nf_o$ = 2*614400 = 1.2288 MHz. It was decided also in this implementation to make the reference clock the same as the I/D circuit input clock (i.e. $Mf_o = 2Nf_o$ = 1.2288 MHz) as it is excepted practice to do so and it makes for easier calculations when determining the DPLL's characteristics. As stated above the characteristics of the DPLL are determined by the value of K and the reference frequency, as $Mf_o = 2Nf_o$ the hold range $\pm \Delta f_h$ simply becomes $f_o/2K$ and also the DPLL's Q factor = $\pi K/k_d$ where k_d is the gain factor of the phase detector, for the ECPD is it 2. The only characteristic of DATA Class 3 processing that is specified within EUROCOM (D/1) is that the tolerance of the DATA baud rate shall not exceed 1 part in 10^4 (i.e. 2400 ± 0.21 Hz) which means that the DPLL may have a very narrow hold range. EUROCOM (D/1) also specifies, for synchronisation purposes (i.e. so as to gain lock) that a 200ms 'Pre-amble' shall be sent prior to any data transmission. The 'pull-in time' of the DPLL to a phase step is $\tau = K/k_d f_o$, however if τ is made ≤ the time between phase steps (i.e. the DPLL responds to every phase step) the output DPLL clock will have a large amount of jitter. Therefore so as to remove the jitter it is better to make τ >> the time between the phase steps, in that the DPLL

responds to and locks on to the average of the phase steps.
Once the DPLL has gained lock by averaging the phase steps, any phase step there after produces little or no change to the output clock, except when the phase step is so great as to exceed the lock range. For the above reason it was necessary to choose a value of K, as from the above formulae it can be seen that the value of K is the primary controlling factor in determining the characteristics of the DPLL, that resulted in a 'pull-in time' of < 200ms, and therefore a value of 512 was chosen. Using the K value of 512 the 'pull-in time' τ = K/2*2400 = 512/4800 = 106ms, the hold range $\pm \Delta f_h$ = 2400/2K = 2400/1024 = $\pm$ 2.3 Hz, the Q factor = 3.142K/2 = 804. Although the hold range is greater than is necessary in accordance with the DATA baud rate tolerance specified in EUROCOM (D/1) any further narrowing of the above hold range by making K = 1024, results in the 'pull-in time' exceeding 200ms and in any case experimental testing showed that increasing K above the value of 512 produced no significant improvement in the output jitter.
The above described configuration, with the exception that both phase detectors were used to give better ripple cancellation on the output frequency, was able to produce an output frequency of 2.4 kHz $\pm$ 2.3 Hz, with a measured ripple, (i.e. jitter), content of between 1-2%, referenced to the original DTE Transmitted Data, in the presence of a bearer circuit error rate of 1 in 10^2.

3.1.4 Pre-amble

It is specified in EUROCOM (D/1) that the DTE shall transmit "a pre-amble of at least 200ms before any data transmission". This pre-amble is intended for use by the DATA Class 3 clock recovery circuit so that it can gain both phase and frequency lock before the arrival of the true data. In the case of synchronous data transmission this pre-amble could well be for example the 'SYN' character which precedes and follows the true data field. This design also requires some form of pre-amble however experimental work was carried out to see whether the need for this pre-amble could be removed by the introduction of a Buffer circuit.

3.1.5 Buffer Circuit

The intention of a Buffer circuit was to provided a delay in the form of data storage to enable the DPLL's output clock to gain both frequency and phase lock with the incoming data before it was used to clock re-stored data onto and out of the Sampler. The Buffer Circuit used in the experiment primarily took the form of a First-In First-Out (FIFO) device. It operated such that the re-sampled RMVD output signal was clocked into the FIFO input using the trailing edge of the 208.33us pulse generated by the Counter circuit. The RMVD output signal is clocked using this signal edge because it represents the nominal timing point from the transition edge of a normal 2.4 kbit/s data bit period of 416.66us and as the minimum RMVD output signal bit period is four times that of the 16 kbit/s bit period, (i.e. 250us), this point always represents the same logic level as that of the original Transmitted Data. When the FIFO becomes approximately half full, in which time the DPLL has gained lock, the DPLL output clock is allowed to clock the stored data out of the FIFO and onto the Sampler. This experiment proved that in principle it is not necessary to transmit a pre-amble before the true data

By making use of such a Buffer Circuit idea and some additional circuitry it is considered possible to use the DPLL in a DATA Class 2 processing configuration, using an ansiochronous data structure, (i.e. Start-Stop), so as to be able to improve the jitter seen on the recovered DATA Class 2 RMVD signal. However this implementation was not fully explored as it is not a required within EUROCOM (D/1). Therefore it is recommended that such a possible implementation be looked if the requirement arises.

4 CONCLUSIONS

With the development of the DATA Class 3 Clock Recovery circuit described in this report, it has been proven that it is possible to regenerate a stable 2.4 kHz timing clock from the regenerated 2.4 kbit/s RMVD output signal.

The use of the DPLL in the clock recover circuit has resulted in the jitter content on the DATA being reduced by upto a factor of ten in an non-errored environment and upto a factor of forty in an errored environment.

5 RECOMMENDATIONS

It is recommended, if required, to investigate fully the possibility of employing this circuit in a DATA Class 2 processing configuration, using an anisochronous data structure, (i.e. Start Stop), with the addition of a Buffer Circuit so as to produce similar jitter improvement as that for the DATA Class 3. Special consideration should be applied to the problem of continuous large phase steps due to the long random 'silent' (i.e. no data transitions) intervals associated with Start-Stop data.

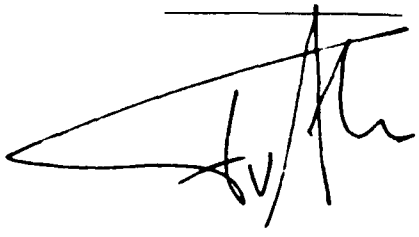
6 REFERENCES

[1]: EUROCOM Tactical Communications Systems,
Basic Parameters (D/1),
September 1986 (Frozen).

[2]: Wim Rosink, 'All-digital phase-locked loops
using the 74HC/HCT297', Electronic Components
and Applications, Vol.9 No.2 pp 66-89.

LIST OF ABBREVIATIONS

BER	Bit Error Rate
DCE	Data Circuit Terminating Equipment
DPLL	Digital Phase-Locked Loop
DTE	Data Terminating Equipment
FEC	Forward Error Correction
FEL	Fysisch en Elektronisch Laboratorium
FIFO	First-In First-Out
I/D	Increment/Decrement
ITA5	International Alphabet No. 5
MSMV	Multiple Sampling and Majority Voting
MSMV&R	Multiple Sampling and Majority Voting and Regeneration
RMVD	Running Majority Voting Detector
TNN	Trunk Node Network
TNO	Organisatie voor Toegepast Natuurwetenschappelijk Onderzoek



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15. ABSTRACT (MAXIMUM 200 WORDS, 1044 POSITIONS)
THIS REPORT DESCRIBES THE DEVELOPMENT OF A EUROCOM DATA CLASS 3, CLOCK RECOVERY IMPLEMENTATION, AS PART OF FEL/TNO'S SUPPORT TO THE ROYAL NETHERLANDS ARMY (RNLA), ZODIAC PROJECT. THE DESIGN CENTRES AROUND THE USE OF A DIGITAL PHASE LOCKED LOOP (DPLL) WHICH RECOVERS A STABLE 2.4 KHZ CLOCK WITH ONLY A JITTER CONTENT OF 1%, FROM THE RECEIVED MULTI-SAMPLED MAJORITY VOTED SIGNAL IN THE PRESENCE OF A BEARER CIRCUIT ERROR RATE OF 1 IN 10^2, AS SPECIFIED IN EUROCOM (D/1).

16. DESCRIPTORS
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COMMUNICATION NETWORKS
DATA TRANSMISSION
ERROR DETECTING CODES
ERROR CORRECTING CODES

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